Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 3, 4, 15, 16, 30, 31, 44, 45, 52-54, 60 and 61, amend claims 1, 13, 28, 43, 46, 47 and 51, and add new claims 62-74 as follows:

Listing of Claims:

1. (Currently Amended) A memory module, comprising:

a plurality of memory devices arranged in a ~~plurality of~~ four ranks; and

a memory hub coupled to the memory devices in each of the ranks, the memory hub being programmable to configure the memory module in each of a plurality of modes ~~data formats each corresponding to a respective number of ranks of memory devices that are simultaneously accessed~~, the memory hub being structured to simultaneously address all four ranks of memory devices in a first mode to simultaneously couple data to or from all of the memory devices in the memory module, to simultaneously address two ranks of memory devices in a second mode to simultaneously couple data to or from the memory devices in the two addressed ranks, or to address one rank of memory devices in a third mode to couple data to or from the memory devices in the addressed rank.

2. (Original) The memory module of claim 1 wherein the memory hub is coupled to the memory devices in each of the ranks through respective busses.

3. (Cancelled)

4. (Cancelled)

5. (Original) The memory module of claim 1, further comprising a programmable storage device coupled to the memory hub, the programmable storage device being programmed to control the operating mode of the memory hub.

6. (Original) The memory module of claim 1 wherein the memory devices in each rank are collectively operable to read or write N-bit data words, and wherein the memory hub further comprises an input/output port that is operable to receive or transmit M*N-bit data words, where M is the number of ranks of memory devices in the memory module.

7. (Original) The memory module of claim 1 wherein the memory devices in each rank are collectively operable to read or write N-bit data words in a first period of time, and wherein the memory hub further comprises an input/output port that is operable to receive or transmit M*N data bits in the first period of time, where M is the number of ranks of memory devices in the memory module.

8. (Original) The memory module of claim 7 wherein the memory devices are operable to read or write data at a rate of X bits per second, and wherein the input/output port comprises an N-bit input/output port that is operable to transmit or receive N-bit data words at a rate of M*X data words per second.

9. (Original) The memory module of claim 7 wherein the memory devices are operable to read or write data at a rate of X bits per second, and wherein the input/output port comprises a 2*N-bit input/output port that is operable to transmit or receive 2*N-bit data words at a rate of M*X/2 data words per second.

10. (Original) The memory module of claim 7 wherein the memory devices are operable to read or write data at a rate of X bits per second, and wherein the input/output port comprises a M*N-bit input/output port that is operable to transmit or receive M*N-bit data words at a rate of X data words per second.

11. (Original) The memory module of claim 1 wherein the memory devices comprise dynamic random access memory devices.

12. (Original) The memory module of claim 11 wherein the dynamic random access memory devices comprise synchronous dynamic random access memory devices.

13. (Currently Amended) A memory system, comprising:

a controller operable to receive a memory request and to transmit a corresponding memory request to an input/output port;

a plurality of memory modules, each of the memory modules comprising:

a plurality of memory devices arranged in ~~a plurality of~~ four ranks; and

a memory hub operable to receive a memory request at an input/output port, the memory hub being coupled to the memory devices in each of the ranks, the memory hub being programmable to configure the memory module in a plurality of modes, the memory hub being structured to simultaneously address all of four ranks of memory devices in a first mode to simultaneously couple data to or from all of the memory devices in the memory module, to simultaneously address two ranks of memory devices in a second mode to simultaneously couple data to or from the memory devices in the two addressed ranks, or to address one rank of memory devices in a third mode to couple data to or from the memory devices in the addressed rank ~~data formats each corresponding to a respective number of ranks of memory devices that are simultaneously accessed~~; and

a communications link coupling the input/output port of the controller to the input/output ports of the memory hubs in the respective memory modules.

14. (Original) The memory system of claim 13 wherein the memory hub in each of the memory modules is coupled to the memory devices in each of the ranks through respective busses.

15. (Cancelled)

16. (Cancelled)

17. (Original) The memory system of claim 13, further comprising a programmable storage device coupled to the memory hub, the programmable storage device being programmed to control the operating mode of the memory hub.

18. (Original) The memory system of claim 13 wherein the memory devices in each rank are collectively operable to read or write N-bit data words, and wherein the memory hub further comprises an input/output port that is operable to receive or transmit M*N-bit data words, where M is the number of ranks of memory devices in the memory module.

19. (Original) The memory system of claim 13 wherein the memory devices in each rank are collectively operable to read or write N-bit data words in a first period of time, and wherein the memory hub further comprises an input/output port that is operable to receive or transmit M*N data bits in the first period of time, where M is the number of ranks of memory devices in the memory module.

20. (Original) The memory system of claim 19 wherein the memory devices are operable to read or write data at a rate of X bits per second, and wherein the input/output port comprises an N-bit input/output port that is operable to transmit or receive N-bit data words at a rate of M*X data words per second.

21. (Original) The memory system of claim 19 wherein the memory devices are operable to read or write data at a rate of X bits per second, and wherein the input/output port comprises a 2*N-bit input/output port that is operable to transmit or receive 2*N-bit data words at a rate of M*X/2 data words per second.

22. (Original) The memory system of claim 19 wherein the memory devices are operable to read or write data at a rate of X bits per second, and wherein the input/output port comprises a M*N-bit input/output port that is operable to transmit or receive M*N-bit data words at a rate of X data words per second.

23. (Original) The memory system of claim 13 wherein the memory devices comprise dynamic random access memory devices.

24. (Original) The memory system of claim 23 wherein the dynamic random access memory devices comprise synchronous dynamic random access memory devices.

25. (Original) The memory system of claim 13 wherein the memory hubs in at least two of the memory modules are programmed to configure the memory module in different data formats.

26. (Original) The memory system of claim 25 wherein the memory hub in a first of the memory modules is programmed to configure the first memory module so that all of the ranks of memory devices in the first memory module are simultaneously addressed, the memory hub in a second of the memory modules is programmed to configure the second memory module so that half of the ranks of memory devices in the second memory module are simultaneously addressed, and the memory hub in a third of the memory modules is programmed to configure the third memory module so that each of the ranks of memory devices in the third memory module are individually addressed.

27. (Original) The memory system of claim 13 wherein the input/output port of the controller and the input/output port of each of the memory hubs comprises an optical input/output port, and wherein the communications link comprises an optical communications link.

28. (Currently Amended) A computer system, comprising:

a central processing unit ("CPU");

a system controller coupled to the CPU, the system controller being operable to receive a memory request from the central processing unit and to transmit a corresponding memory request to an input/output port;

an input device coupled to the CPU through the system controller;

an output device coupled to the CPU through the system controller;

a storage device coupled to the CPU through the system controller;

a plurality of memory modules, each of the memory modules comprising:

a plurality of memory devices arranged in ~~a plurality of~~ four ranks; and

a memory hub operable to receive a memory request at an input/output port, the memory hub being coupled to the memory devices in each of the ranks, the memory hub being programmable to configure the memory module in a plurality of ~~data~~

~~formats each corresponding to a respective number of ranks of memory devices that are simultaneously accessed~~ modes, the memory hub being structured to simultaneously address all of four ranks of memory devices in a first mode to simultaneously couple data to or from all of the memory devices in the memory module, to simultaneously address two ranks of memory devices in a second mode to simultaneously couple data to or from the memory devices in the two addressed ranks, or to address one rank of memory devices in a third mode to couple data to or from the memory devices in the addressed rank; and

a communications link coupling the input/output port of the system controller to the input/output ports of the memory hubs in the respective memory modules.

29. (Original) The computer system of claim 28 wherein the memory hub in each of the memory modules is coupled to the memory devices in each of the ranks through respective busses.

30. (Cancelled)

31. (Cancelled)

32. (Original) The computer system of claim 28, further comprising a programmable storage device coupled to the memory hub, the programmable storage device being programmed to control the operating mode of the memory hub.

33. (Original) The computer system of claim 28 wherein the memory devices in each rank are collectively operable to read or write N-bit data words, and wherein the memory hub further comprises an input/output port that is operable to receive or transmit M*N-bit data words, where M is the number of ranks of memory devices in the memory module.

34. (Original) The computer system of claim 28 wherein the memory devices in each rank are collectively operable to read or write N-bit data words in a first period of time, and wherein the memory hub further comprises an input/output port that is operable to receive or

transmit M*N data bits in the first period of time, where M is the number of ranks of memory devices in the memory module.

35. (Original) The computer system of claim 34 wherein the memory devices are operable to read or write data at a rate of X bits per second, and wherein the input/output port comprises an N-bit input/output port that is operable to transmit or receive N-bit data words at a rate of M*X data words per second.

36. (Original) The computer system of claim 34 wherein the memory devices are operable to read or write data at a rate of X bits per second, and wherein the input/output port comprises a 2*N-bit input/output port that is operable to transmit or receive 2*N-bit data words at a rate of M*X/2 data words per second.

37. (Original) The computer system of claim 34 wherein the memory devices are operable to read or write data at a rate of X bits per second, and wherein the input/output port comprises a M*N-bit input/output port that is operable to transmit or receive M*N-bit data words at a rate of X data words per second.

38. (Original) The computer system of claim 28 wherein the memory devices comprise dynamic random access memory devices.

39. (Original) The computer system of claim 38 wherein the dynamic random access memory devices comprise synchronous dynamic random access memory devices.

40. (Original) The computer system of claim 28 wherein the memory hubs in at least two of the memory modules are programmed to configure the memory module in different data formats.

41. (Original) The computer system of claim 40 wherein the memory hub in a first of the memory modules is programmed to configure the first memory module so that all of the ranks of memory devices in the first memory module are simultaneously addressed, the

memory hub in a second of the memory modules is programmed to configure the second memory module so that half of the ranks of memory devices in the second memory module are simultaneously addressed, and the memory hub in a third of the memory modules is programmed to configure the third memory module so that each of the ranks of memory devices in the third memory module are individually addressed.

42. (Original) The computer system of claim 28 wherein the input/output port of the system controller and the input/output port of each of the memory hubs comprises an optical input/output port, and wherein the communications link comprises an optical communications link.

43. (Currently Amended) A method of accessing data in a memory module containing a plurality of memory devices, the method comprising:

dividing the memory devices into ~~a plurality of~~ M ranks, where M is a positive greater than or equal to four;

configuring the memory module to access the data stored in the memory module in a first data format in which ~~a first number of~~ M ranks of memory devices are simultaneously accessed; ~~and~~

configuring the memory module to access the data stored in the memory module in a second data format in which ~~a second number of~~ M/2 ranks of memory devices are simultaneously accessed~~, the second number being different from the first~~; and

configuring the memory module to access the data stored in the memory module in a third data format in which one rank of memory devices is simultaneously accessed.

44. (Cancelled)

45. (Cancelled)

46. (Currently Amended) The method of claim 43 wherein the memory devices in each rank are collectively operable to read or write N-bit data words, and wherein the

method further comprises receiving or transmitting M*N-bit data words from the memory module~~, where M is the number of ranks of memory devices in the memory module~~.

47. (Currently Amended) The method of claim 43 wherein the memory devices in each rank are collectively operable to read or write N-bit data words in a first period of time, and wherein the method further comprises receiving at the memory module or transmitting from the memory module M N-bit data bits in the first period of time~~, where M is the number of ranks of memory devices in the memory module~~.

48. (Original) The method of claim 47 wherein the memory devices in the memory module are operable to read or write data at a rate of X bits per second, and wherein the method further comprises receiving at the memory module or transmitting from the memory module N-bit data words data at a rate of M*X data words per second.

49. (Original) The method of claim 47 wherein the memory devices in the memory module are operable to read or write data at a rate of X bits per second, and wherein the method further comprises receiving at the memory module or transmitting from the memory module 2*N-bit data words data at a rate of M*X/2 data words per second.

50. (Original) The method of claim 47 wherein the memory devices in the memory module are operable to read or write data at a rate of X bits per second, and wherein the method further comprises receiving at the memory module or transmitting from the memory module M*N-bit data words data at a rate of X data words per second.

51. (Currently Amended) In a computer system, a method of accessing data in a plurality of memory modules each of which contains a plurality of memory devices, the method comprising:

dividing the memory devices in each of the memory modules into a plurality of ranks;

configuring each of the memory modules to access the data stored in the memory module in one of a plurality of data formats each corresponding to a respective number of ranks

of memory devices that are simultaneously accessed, a first of the memory modules being configured so that so that all of the ranks of memory devices in the first memory module are simultaneously addressed, a second of the memory modules being configured so that so that half of the ranks of memory devices in the second memory module are simultaneously addressed, and a third of the memory modules being configured so that so that each of the ranks of memory devices in the third memory module are individually addressed; and

accessing data in each of the memory modules in the configured data format.

52. (Cancelled)

53. (Cancelled)

54. (Cancelled)

55. (Original) The method of claim 51 wherein the memory devices in each rank are collectively operable to read or write N-bit data words, and wherein the method further comprises receiving or transmitting M*N-bit data words from each of the memory modules, where M is the number of ranks of memory devices in the memory module.

56. (Original) The method of claim 51 wherein the memory devices in each rank are collectively operable to read or write N-bit data words in a first period of time, and wherein the method further comprises receiving at each of the memory modules or transmitting from each of the memory modules M N-bit data bits in the first period of time, where M is the number of ranks of memory devices in the memory module.

57. (Original) The method of claim 56 wherein the memory devices in each of the memory modules are operable to read or write data at a rate of X bits per second, and wherein the method further comprises receiving at each of the memory modules or transmitting from each of the memory modules N-bit data words data at a rate of M*X data words per second.

58. (Original) The method of claim 56 wherein the memory devices in each of the memory modules are operable to read or write data at a rate of X bits per second, and wherein the method further comprises receiving at each of the memory modules or transmitting from each of the memory modules 2*N-bit data words data at a rate of M*X/2 data words per second.

59. (Original) The method of claim 56 wherein the memory devices in each of the memory modules are operable to read or write data at a rate of X bits per second, and wherein the method further comprises receiving at each of the memory modules or transmitting from each of the memory modules M*N-bit data words data at a rate of X data words per second.

60. (Cancelled)

61. (Cancelled)

62. (New) A memory module, comprising:

a plurality of memory devices arranged in a plurality of M ranks each having an N-bit data bus, the memory devices being operable to read or write data at a rate of X bits per second; and

a memory hub coupled to the memory devices in each of the ranks, the memory hub being programmable to configure the memory module in a plurality of data formats each corresponding to a respective number of ranks of memory devices that are simultaneously accessed, the memory hub further including an N*P-bit input/output port that is operable to receive or transmit M*N data bits in N*P-bit words at a rate of (M*X)/P data words per second, where N and P are respective positive integers.

63. (New) The memory module of claim 62 wherein the memory hub is coupled to the memory devices in each of the ranks through respective busses.

64. (New) The memory module of claim 62, further comprising a programmable storage device coupled to the memory hub, the programmable storage device being programmed to control the operating mode of the memory hub.

65. (New) The memory module of claim 62, wherein M=4 and P=4 such that the input/output port comprises an 4*N-bit input/output port that is operable to receive or transmit 4*N data bits in 4*N-bit words at a rate of X data words per second.

66. (New) A memory system, comprising:

a controller operable to receive a memory request and to transmit a corresponding memory request to an input/output port;

a plurality of memory modules, each of the memory modules comprising:

a plurality of memory devices arranged in a plurality of M ranks each having an N-bit data bus, the memory devices being operable to read or write data at a rate of X bits per second;

a memory hub coupled to the memory devices in each of the ranks, the memory hub being programmable to configure the memory module in a plurality of data formats each corresponding to a respective number of ranks of memory devices that are simultaneously accessed, the memory hub further including an N*P-bit input/output port that is operable to receive or transmit M*N data bits in N*P-bit words at a rate of (M*X)/P data words per second, where N and P are respective positive integers; and

a communications link coupling the input/output port of the controller to the input/output ports of the memory hubs in the respective memory modules.

67. (New) The memory system of claim 66 wherein the memory hub is coupled to the memory devices in each of the ranks through respective busses.

68. (New) The memory system of claim 66, further comprising a programmable storage device coupled to the memory hub, the programmable storage device being programmed to control the operating mode of the memory hub.

69. (New) The memory system of claim 66, wherein M=4 and P=4 such that the input/output port comprises an 4*N-bit input/output port that is operable to receive or transmit 4*N data bits in 4*N-bit words at a rate of X data words per second.

70. (New) A computer system, comprising:

a central processing unit ("CPU");

a system controller coupled to the CPU, the system controller being operable to receive a memory request from the central processing unit and to transmit a corresponding memory request to an input/output port;

an input device coupled to the CPU through the system controller;

an output device coupled to the CPU through the system controller;

a storage device coupled to the CPU through the system controller;

a plurality of memory modules, each of the memory modules comprising:

a plurality of memory devices arranged in a plurality of M ranks each having an N-bit data bus, the memory devices being operable to read or write data at a rate of X bits per second;

a memory hub coupled to the memory devices in each of the ranks, the memory hub being programmable to configure the memory module in a plurality of data formats each corresponding to a respective number of ranks of memory devices that are simultaneously accessed, the memory hub further including an N*P-bit input/output port that is operable to receive or transmit M*N data bits in N*P-bit words at a rate of (M*X)/P data words per second, where N and P are respective positive integers; and

a communications link coupling the input/output port of the system controller to the input/output ports of the memory hubs in the respective memory modules.

71. (New) The computer system of claim 70 wherein the memory hub in each of the memory modules is coupled to the memory devices in each of the ranks through respective busses.

72. (New) The computer system of claim 70, further comprising a programmable storage device coupled to the memory hub, the programmable storage device being programmed to control the operating mode of the memory hub.

73. (New) A computer system, comprising:

a central processing unit ("CPU");

a system controller coupled to the CPU, the system controller being operable to receive a memory request from the central processing unit and to transmit a corresponding memory request to an input/output port;

an input device coupled to the CPU through the system controller;

an output device coupled to the CPU through the system controller;

a storage device coupled to the CPU through the system controller;

a plurality of memory modules, each of the memory modules comprising:

a plurality of memory devices arranged in a plurality of ranks; and

a memory hub operable to receive a memory request at an input/output port, the memory hub being coupled to the memory devices in each of the ranks, the memory hub being programmable to configure the memory module in a plurality of data formats each corresponding to a respective number of ranks of memory devices that are simultaneously accessed, the memory hub in a first of the memory modules being programmed to configure the first memory module so that all of the ranks of memory devices in the first memory module are simultaneously addressed, the memory hub in a second of the memory modules being programmed to configure the second memory module so that half of the ranks of memory devices in the second memory module are simultaneously addressed, and the memory hub in a third of the memory modules being programmed to configure the third memory module so that each of the ranks of memory devices in the third memory module are individually addressed; and

a communications link coupling the input/output port of the system controller to the input/output ports of the memory hubs in the respective memory modules.

74. (New) In a computer system, a method of accessing data in a plurality of memory modules each of which contains a plurality of memory devices, the method comprising:

dividing the memory devices in each of the memory modules into M ranks each of which has an N-bit data bus, the memory devices being operable to read or write data at a rate of X bits per second;

configuring each of the memory modules to access the data stored in the memory module in one of a plurality of data formats each corresponding to a respective number of ranks of memory devices that are simultaneously accessed, each of the memory modules being configured to receive or transmit M*N data bits in N*P-bit words at a rate of (M*X)/P data words per second, where N and P are respective positive integers; and

accessing data in each of the memory modules in the configured data format.